GENERAL DESIGN GUIDE LINES

CONDUCTORS	Minimum Line Width / Minimum Space Width	12.5 um
	Line Width Tolerance	5 um Standard 2.5 um Select
	Space Tolerance	5 um Standard 2.5 um Select
	Minimum Pad Size Around VIA (D : hole diameter)	250 um + D
RESISTORS	Nominal Tolerance	5%
	Minimum Spacing Between Resistors	50 um
	Minimum Length and / or Width	50 um
	Nominal Sheet Resistance (ohms/□) Preferred Sheet Resistance (ohms/□)	10 – 200 50 or 100
METALIZED HOLES (VIA'S)	Minimum Aspect Ratio (Hole diameter: Substrate thickness)	0.6:1
	Minimum Tolerance	50 um
	Minimum Distance from Hole Circumference To Edge (T : substrate thickness) or adjacent hole circumference	T
	Minimum True Center Tolerance	25 um
SUBSTRATES	Thickness Tolerance	±10 %
	Minimum Length / Width Tolerance	25 um
	Surface Finish (Microinch – CLA not available in all materials)	< 100 nm
	Typical Camber	0.3%
DATA FORMAT	DXF, DWG Traces: Closed Polylines (0 Width)	
	Minimum Resistor On Conductor Overlap	50 um

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